The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by ~~a first~~ an upper end surface, a ~~second~~ lower end surface opposing to the ~~first~~ upper end surface, and first and second side boundary surfaces connecting the ~~first and second~~ upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type being in metallurgical contact with said first semiconductor region at the ~~second~~ lower end surface;

a third semiconductor region of a second conductivity type being in metallurgical contact with said first semiconductor region at the ~~first~~ upper end surface; and

a fourth semiconductor region having first and second inner surfaces in metallurgical contact with the first and second side boundary surfaces respectively when viewed in section and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions.

2. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region has the first conductivity type.

3. (Currently amended) The semiconductor device of Claim 1, wherein outer surface of said fourth semiconductor region serves as a chip outer-surface of the semiconductor device and the chip outer-surface is substantially orthogonal with the ~~second~~ lower end surface of said first semiconductor region.

4. (Original) The semiconductor device of Claim 1, wherein said fourth semiconductor region is made of a wafer cut from bulk crystal.

5. (Previously amended) The semiconductor device of Claim 1, further comprising a first main electrode layer formed on a bottom surface of said second semiconductor region.

6. (Previously presented) The semiconductor device of Claim 5, wherein said first main electrode layer is contacted with said second semiconductor region, through a first concavity formed at the bottom surface of said semiconductor region.

7. (Previously presented) The semiconductor device of Claim 1, further comprising a first main electrode layer, a part of the first main electrode layer being buried in a via hole penetrating through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said first semiconductor region.

8. (Previously presented) The semiconductor device of Claim 1, further comprising a second main electrode layer formed on a top surface of said third semiconductor region.

9. (Previously presented) The semiconductor device of Claim 8, wherein said second main electrode layer is contacted with said third semiconductor region, through a second concavity formed at the top surface of said third semiconductor region.

10. (Cancelled).

11. (Cancelled).

12. (Currently amended) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by ~~a first~~ an upper end surface, a ~~second~~ lower end surface opposing to the ~~first~~ upper end surface, and first and second side boundary surfaces connecting the ~~first and second~~ upper and lower end surfaces when viewed in section;

a second semiconductor region of the first conductivity type having first and second upper surfaces when viewed in section;

a third semiconductor region of a second conductivity type being in metallurgical contact with said first semiconductor region at the ~~first~~ upper end surface;

a fourth semiconductor region having first and second inner surfaces in metallurgical contact with the first and second side boundary surfaces respectively when viewed in section and having first and second lower end surfaces in metallurgical contact with said first and second upper surfaces respectively when viewed in section, and an impurity concentration lower than said first semiconductor region, configured such that the fourth semiconductor region is disposed between the second and third semiconductor regions; and

a first main electrode layer, a part of the first main electrode layer being buried through said second semiconductor region, configured such that the buried part of the first main electrode layer contacts with said ~~second~~ lower end surface of said first semiconductor region.

13. (Currently amended) A semiconductor device comprising:

a first semiconductor region of a first conductivity type, defined by ~~a first~~ an upper end surface, a ~~second~~ lower end surface opposing to the ~~first~~ upper end surface and a side boundary surface connecting the ~~first and second~~ upper and lower end surfaces;

a second semiconductor region of the first conductivity type being in metallurgical contact with said first semiconductor region at the ~~second~~ lower end surface;

a third semiconductor region of a second conductivity type being in metallurgical contact with said first semiconductor region at the ~~first~~ upper end surface; and

a fourth semiconductor region having an inner surface in metallurgical contact with the side boundary surface and an impurity concentration lower than said first semiconductor region, configured such that the inner surface of the fourth semiconductor region surrounds the side boundary surface of the first semiconductor region, the fourth semiconductor region being disposed between the second and third semiconductor regions.